A Wear-leveling Method for Balanced Multi-chip Life-time in NAND Flash-based Storage Devices

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***Abstract*—For high performance and large capacity, modern NAND flash-based storage devices (NFSDs) adopt a multi-chip architecture. However, a variety of workloads toward NFSDs induce uneven program/erase count of NAND flash memories (NFMs) which results in an imbalance of life-time of NFMs. In this paper, therefore, we propose a wear-leveling method that improves the life-time of NFSDs by redirecting write requests of an NFM having maximum erase count (E_c) to another NFM having minimum E_c. In this experiment, the proposed method reduces standard deviation of E_c and maximum E_c by 90% and 20%, respectively, which implies that the proposed method improves both the life-time of NFMs and NFSD significantly.**

***Keywords*—NAND flash memory, storage device, wear-leveling, multi-chip architecture**

I. Introduction

Due to many advantages over hard disk drives (HDDs), NAND flash-based storage devices (NFSDs) have been widely used. For high performance and large capacity, modern NFSDs adopt a multi-chip architecture consisting of multiple channels and ways [1]. In this architecture, a variety of workloads toward NFSDs induce uneven program/erase count of NAND flash memories (NFMs) since an NFM may need to handle a larger amount of data than other NFMs, which results in an imbalance of life-time of NFMs.

Since the life-time of an NFSD can be dominated by a single NFM with the shortest life-time and the life-time of an NFM is inversely proportional to its erase count (E_c), it is very important that all NFMs have balanced E_c. Fig. 1 shows E_cs of 8 NFMs in one NFSD, which are normalized by average E_c (avgE_c). NFMs have balanced E_c in TPC, but have two times or more imbalanced E_c in MRS. As a result, wear-out level of an overall NFSD is determined by 2nd NFM.

In this paper, therefore, we propose a wear-leveling method that improves the overall life-time in NFSDs with multi-chip architecture by balancing E_c of every NFM. More specifically, the proposed method monitors E_c of NFMs and redirects write requests from one NFM to another when E_cs of certain NFMs are imbalanced. Although not discussed in this paper, the proposed method can also be utilized to compensate the deviation of life-time occurred by the processing variation of NFMs.

II. Multi-chip wear-leveling

The data flow of the proposed method is shown in Fig. 2. A request given to the NFSD is transferred to a software layer to manage NFMs, called a flash translation layer (FTL), which not only translates a logical address of a request to a physical address but also distributes data to channels and ways [2]. However, data allocation by an existing FTL can cause imbalanced program/erase count because it always delivers data to a predetermined NFM regardless of its wear-out state. Therefore, we propose a wear-leveling method for balanced multi-chip life-time ($BMWL$). The proposed method includes an E_c monitor and a redirection manager considering wear-out state of NFMs.

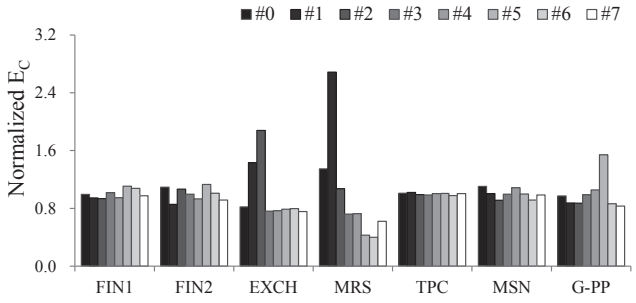

Fig. 1. Normalized erase count of 8 NFMs in one NFSD with multi-chip

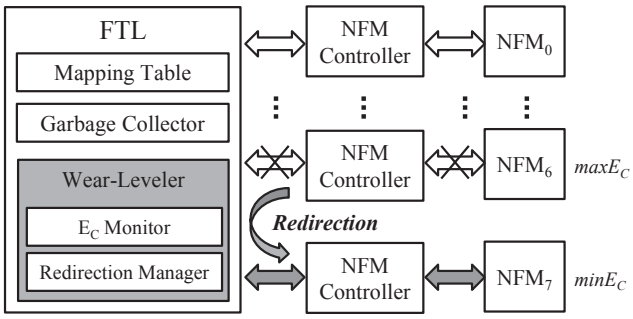

Fig. 2. Data flow of the proposed method

When a write request is given, the E_c monitor checks E_c of each NFM and avgE_c, and then the redirection manager decides whether the write request is to be redirected or not. A redirection is activated when the following two conditions are met, 1) maxE_c is 5% larger than avgE_c and 2) the NFM decided by the FTL has maxE_c. The redirection of write requests from the NFM with maxE_c to the NFM with minE_c is continued until the difference between maxE_c and avgE_c reaches 5%.

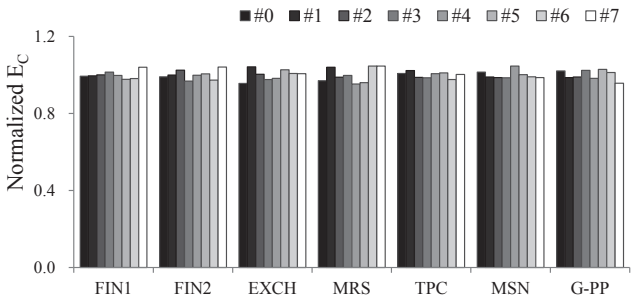

Fig. 3. Normalized erase count (E_C)

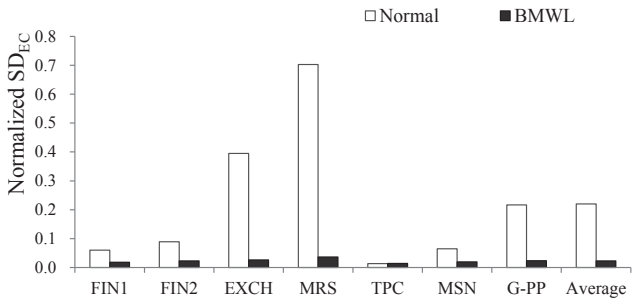

Fig. 4. Standard deviation of normalized erase count (SD_{EC})

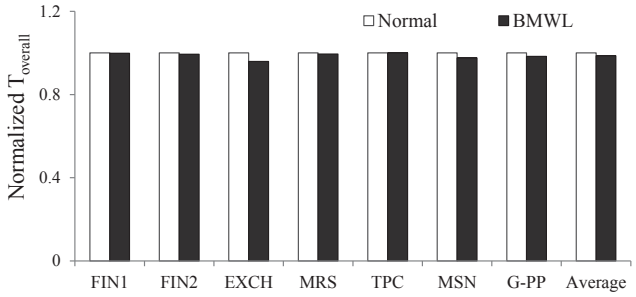

Fig. 5. Normalized overall throughput ($T_{overall}$)

In Fig. 2, we assume that NFM_6 and NFM_7 have maxE_c and minE_c respectively. In this situation, the proposed method redirects the write request, which is originally directed to NFM_6, to NFM_7. If data with same logical page address in NFM_6 exist, the data should be moved to NFM_7 after being temporarily stored in NFM controller, which requires additional time for data transfer. Nevertheless, as shown in the following experiment result, the overhead is negligible thanks to faster data transfer speed and a partial data update of modern NFMs.

III. Evaluation

To evaluate the effectiveness of the proposed method, we implemented a trace-driven simulator that consists of a page-level FTL [3], the specification of NFM [4] and the configurations of storage system. Various workloads are collected from [5] (FIN1, FIN2), [6] (EXCH, MRS, TPC, MSN) and by DiskMon [7] (G-PP) during daily PC use.

Fig. 3, 4 and 5 shows performance of the proposed method, which is compared to the baseline which does not consider multi-chip wear-leveling ($Normal$). As shown in Fig. 3, the proposed $BMWL$ maintains balanced E_c regardless of workloads in contrast Fig. 1. Quantitatively, in Fig. 4, standard deviation of normalized erase count (SD_{EC}) of $BMWL$ is 20 times smaller than $Normal$ in EXCH and MRS. On average, $BMWL$ reduces SD_{EC} and maxE_c by 90% and 20% respectively, which means that the proposed method not only improves the life-time balance of individual NFMs but also improves overall life-time of NFSD.

Fig. 5 shows overall throughput ($T_{overall}$) of $BMWL$ and $Normal$. Although $BMWL$ requires additional data transfer when redirecting write requests, the overhead of $BMWL$ is only 1% for the compensation of significant improvement of life-time. The small overhead comes from faster data transfer speed up to 200MB/s.

IV. Conclusion

This paper proposes a wear-leveling method that improves overall life-time of a NFSD consisting of multiple NFMs. For balanced E_c of all NFMs, the proposed method monitors E_c of multi-chip and redirects write from an imbalanced NFM to another. In experiment, the proposed method greatly improves overall life-time of NFSD through balanced E_c of multi-chip. Additionally, the proposed method can be modified to compensate a deviation of life-time deviation occurred by the processing variation of NFMs.

Acknowledgment

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